WHAT IS CLAIMED IS:

1. A memory cell comprising:

a substrate having an active region defined therein;

a tunnel insulation layer on the active region;

a floating gate disposed on the tunnel insulation layer;

a gate interlayer dielectric layer on the floating gate;

a control gate electrode on the gate interlayer dielectric layer; and

first and second source/drain regions on respective sides of the control gate electrode,

wherein a first one of the active region and the floating gate comprises a portion that protrudes towards a second one of the active region and the floating gate.

2. The memory cell of Claim 1, wherein the protruding portion tapers toward the second one of the active region and the floating gate.

3. The memory cell of Claim 1, wherein the tunnel insulation layer is narrowed at the protruding portion.

4. The memory cell of Claim 1, wherein the active region comprises at least one protruding portion that protrudes toward the floating gate and wherein the floating gate comprises at least one protruding portion that protrudes toward the active region.

5. The memory cell of Claim 1, wherein the protruding portion adjoins the device isolation layer.

6. The memory cell of Claim 5, wherein the protruding portion comprises an elongate, tapered region disposed between the device isolation layer and a planar portion of the first one of the active region and the floating gate.

7. The memory cell of Claim 1, wherein the source/drain regions comprise respective impurity diffusion regions in the substrate.

8. A method of forming a memory cell, comprising:

forming a device isolation layer in and/or on the substrate, the device isolation layer defining an active region on the substrate;

forming a tunnel insulation layer on the active region;

forming a floating gate on the tunnel insulation layer;

forming a gate interlayer dielectric layer on the floating gate;

forming a control gate electrode on the gate interlayer dielectric layer; and

forming first and second source/drain regions on respective sides of the control gate electrode;

wherein a first one of the active region and the floating gate comprises a portion that protrudes towards a second one of the active region and the floating gate.

9. The method of Claim 8, wherein the protruding portion is tapered toward the second one of the active region and floating gate.

10. The method of Claim 8, wherein the tunnel insulation layer is narrowed at the protruding portion.

11. The method of Claim 8, wherein the active region comprises at least one protruding portion that protrudes toward the floating gate and wherein the floating gate comprises at least one protruding portion that protrudes toward the active region.

12. The method of Claim 8:

wherein forming a tunnel insulation layer is preceded by:

forming a spacer on a sidewall of the device isolation layer and in contact with the active region, wherein the spacer has etch selectivity with respect to the active region;

etching the active region using the first spacer as a mask to form a recess in the active region bounded by a protruding portion of the active region underlying the spacer; and

removing the spacer to expose the protruding portion of the active region; and

wherein forming the tunnel insulation layer comprises thermally oxidizing the exposed active region to form the tunnel isolation region and to taper the protruding portion of the active region.

13. The method of Claim 12:

wherein forming a floating gate is preceded by:

forming a spacer on a sidewall of the device isolation layer and in contact with the tunnel insulation layer;

forming a material pattern on the tunnel insulation layer adjacent the spacer; and

etching the spacer, the material pattern and the tunnel insulation layer to expose the tunnel insulation layer and form a tapered groove therein; and

wherein forming a floating gate comprises forming a floating gate that is disposed on the tunnel insulation layer and has a portion the protrudes into the tapered groove.

14. The method of Claim 8:

wherein forming a floating gate is preceded by:

forming a spacer on a sidewall of the device isolation layer and in contact with the tunnel insulation layer;

forming a material pattern on the tunnel insulation layer adjacent the spacer; and

etching the spacer, the material pattern and the tunnel insulation layer to expose the tunnel insulation layer and form a tapered groove therein; and

wherein forming a floating gate comprises forming a floating gate that is disposed on the tunnel insulation layer and has a portion the protrudes into the tapered groove.